DTCA

Dual Thin-Film Capacitors – *Format A*

Features:

- Ultra-low profile (as thin as 0.1mm)
- Topside wire-bonding pads
- Optional backside contact
- High quality LPCVD nitride dielectric
- Superior breakdown voltage performance
- Low ESR & High Q
- Tolerances as low as ±5%
- 100% electrically tested
- Topside passivation for pick and place handling
- RoHS compliant and Pb-free

Applications:

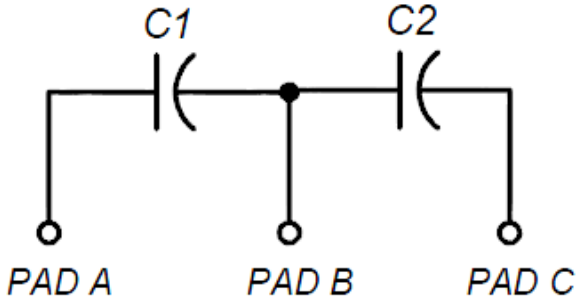
- 13.56 MHz contactless smart cards
- RFID resonance circuits
- Chip-on-Board (COB) designs
- Known Good Die (KGD) programs

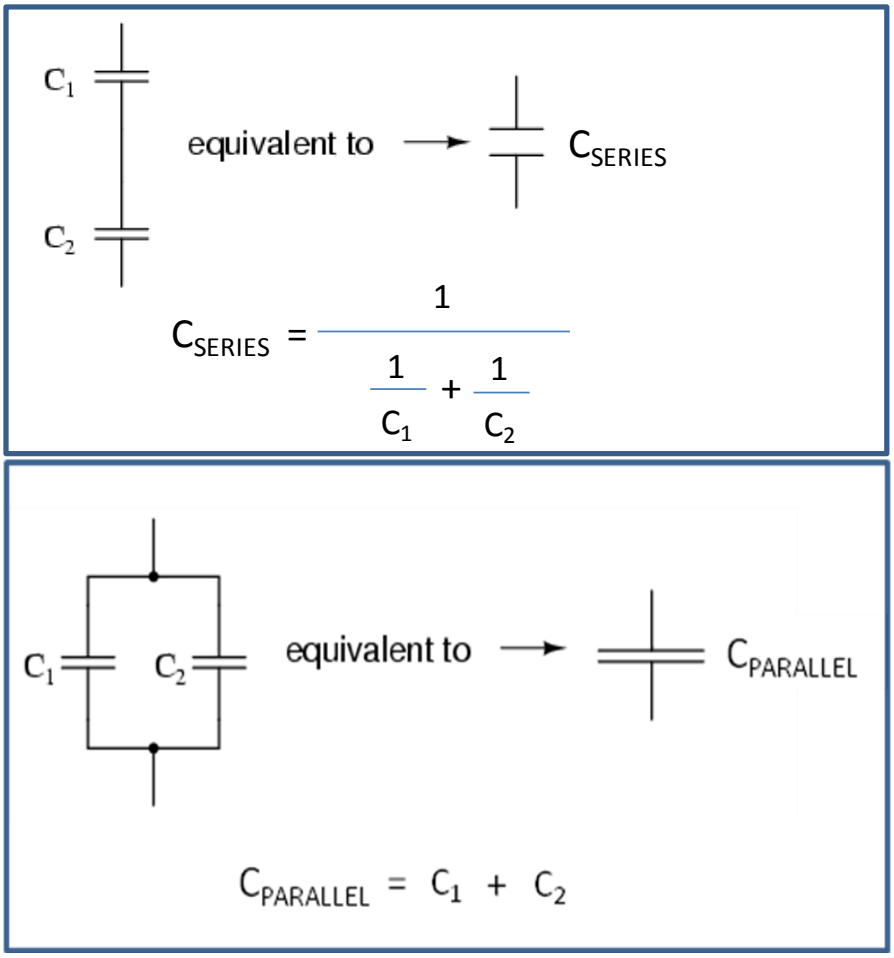
Product Description

OnChip's DTCA dual capacitor chip is designed for RFID applications requiring both a tuning and a detuning capacitance in a single chip. By connecting the internal capacitors either individually or in series or in parallel, the resonant frequency of the LC antenna circuit may easily be varied. As an example, if each capacitor value on the chip is 68pF, when these 2 caps are connected in series, the value will be 34pF and when connect in parallel, the value will be 136pF. The capacitance network is well suited for 13.56MHz ISO 15693 smart card applications, ISO 18000-3 RFID item management tags, and other applications that require precision, high frequency operation, and an ultra-thin profile.

The chip features topside wire bonding pads to support Chip-on-Board (COB) and Direct Chip Attachment (DCA) manufacturing flows. The middle electrical terminal (B) can also be contacted through the substrate if an optional backside gold (Au) metallization flow is selected. Capacitor layout is optimized to reduce effective series resistance (ESR) and to boost quality factor (Q). The entire chip is passivated with a silicon nitride topside layer to protect the die during pick and place handling.

OnChip capacitors use LPCVD silicon nitride as the capacitor dielectric. LPCVD outperforms the plasma-enhanced (PECVD) dielectrics used by other thin-film manufacturers, yielding a film of superior uniformity and electrical breakdown characteristics. The result is a rugged capacitor better suited to the transient voltage conditions of RFID antenna coil applications.





Capacitance (pF)				Capacitance Code	Available Tolerances	Working Voltage (volts)	Breakdown Voltage (volts)
C_1	C_2	C_{SERIES}	$C_{PARALLEL}$				
45	45	22.5	90	045	±5%, ±10% and ±20%	33	49.5
68	68	34	136	068	±5%, ±10% and ±20%	30	45
80	80	40	160	080	±5%, ±10% and ±20%	28	42
100	100	50	200	100	±5%, ±10% and ±20%	25	37.5
165	165	82.5	330	165	±5%, ±10% and ±20%	17	25.5

Electrical Specifications (1)

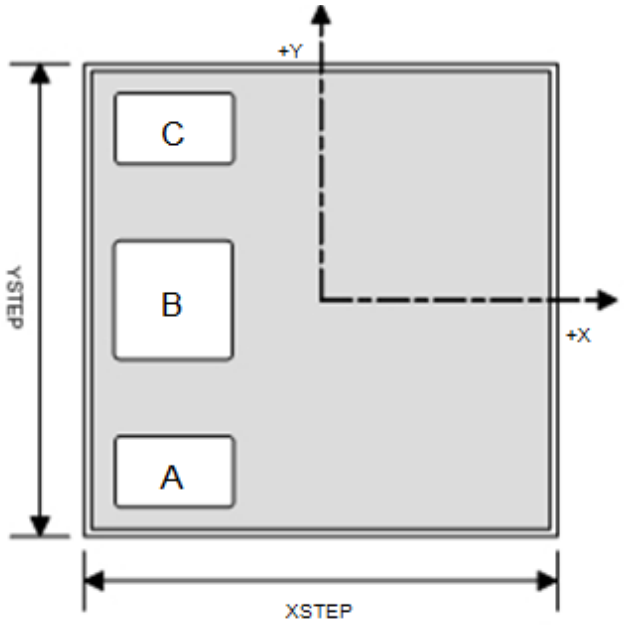
Parameter	Symbol	Conditions
Capacitance	C1, C2	1 MHz, 1 Vrms, 100% electrically tested
Temperature Coefficient of Capacitance	TCC	+45 ±25 ppm/°C
Operating Temperature Range	T_{OP}	-55°C to +125°C
Insulation Resistance	IR	> 10^{10} ohms
Aging	AR	No aging effect
Working Voltage	WV	Maximum continuous operating voltage
Breakdown Voltage	V_{BR}	> 1.5 X Working Voltage

(1) All measurements at 25°C unless otherwise specified

ORDERING PART NUMBER					
DTCA	330	K	7	A	W
Product Family	Value of each Capacitor (C1 & C2)	Capacitor Tolerance	Device Thickness	Back Metal for Die Attach (Typical thickness)	Package Type
	Capacitance Code Examples: 068 = 68pF and 330 = 330pF	J = ±5%	9 = 9 mils	No Letter = Bare Silicon (No Back Metal)	W = Unsawn full 5" wafer
		K = ±10%	7 = 7 mils	A= Ti/Ni/Au (550A/4,000A/2,500A)	B = Diced and shipped on mylar/tape in Saw rings
		M = ±20%	6 = 6 mils	S = Ti/Ag (550A/5,000A)	P = Diced and shipped in Gelpak

Part Number *Example: DTCA068K6AW is an OnChip Dual Capacitor; 68pF ±10%; 6-mils thick with Ti/Ni/Au back-metal and shipped as unsawn wafer*

Chip Layout & Pad Locations



Bond Pad Coordinates	Connection	Parameter	X	Y	Units
Pad A	C1 Electrode	Center of Bond Pad (3)	-310	-363	Microns
		Width of Passivation Opening	250	150	Microns
Pad B	C1 / C2 Shared Electrode + Substrate Connection	Center of Bond Pad (3)	-312	0	Microns
		Width of Passivation Opening	250	250	Microns
Pad C	C2 Electrode	Center of Bond Pad (3)	-310	363	Microns
		Width of Passivation Opening	250	150	Microns

Pad locations referenced to the center of the die. The +Y direction is away from the wafer flat

Physical Dimensions			
Parameter	Symbol	Dimension	Units
Capacitor Length (typical) (Note)	L	0.95 / (0.0374)	mm / (inches)
Capacitor Width (typical) (Note)	W	0.95 / (0.0374)	mm / (inches)
Capacitor Thickness	T	0.23-0.13 / (0.009-0.005)	mm / (inches)
Die Stepping Distance on Wafer in X Direction	XSTEP	1,000	microns
Die Stepping Distance on Wafer in Y Direction	YSTEP	1,000	Microns

Note: Final L, W dimensions depend on conditions and equipment used for wafer sawing. Values shown above reflect a 50 micron wide saw kerf.